

PTH03020 3.3Vin Single

Application Note 151

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1. Introduction

The PTH family of non-isolated, wide-output adjust power modules from Artesyn Technologies are optimized for applications that require a flexible, high performance module that is small in size. These products are part of the "Point-of-Load Alliance" (POLA), which ensures compatible footprint, interoperability and true second sourcing for customer design flexibility. The POLA is a collaboration between Artesyn Technologies, Astec Power and Texas Instruments to offer customers advanced non-isolated modules that provide the same functionality and form factor. Product series covered by the alliance includes the PTHxx050W (6 A), PTHxx060W (10 A), PTHxx010W (15/12 A), PTHxx020W (22/18 A), and the PTHxx030W (30/26 A).

From the basic, "Just Plug it In" functionality of the 6 A modules, to the 30 A rated feature-rich PTHxx030W, series these products were designed to be very flexible, yet simple to use. The features vary with each product series. Table 1 provides a quick reference to the available features by series and input bus voltage.

For simple point-of-use applications, the PTHxx050W series provides operating features such as an ON/OFF inhibit, output voltage trim, pre-bias start-up (3.3/5 V input only), and overcurrent protection. The PTHxx060W (10 A), and PTHxx010W (15/12 A) series add an output voltage sense, and margin up/down controls. The higher output current, PTHxx020W and PTHxx030W series also incorporates overtemperature and shutdown protection. All of the products referenced in Table 1 include Auto-TrackTM.

This is a feature unique to the PTH family, and was specifically designed to simplify the task of sequencing the supply voltage in a power system. These and other features are described in the following sections.

SERIES	INPUT BUS	I _{OUT}	ADJUST TRIM	ON/OFF INHIBIT	OVER- CURRENT	PRE-BIAS STARTUP	AUTO- TRACK™*	MARGIN UP/DOWN	OUTPUT SENSE	THERMAL SHUTDOWN
PTHxx050	3.3 V 5 V 12 V	6 A 6 A 6A	•	•	•	•	•			
PTHxx060	3.3 V/5 V 12 V	10 A 10 A	•	•	•	•	•	•	•	
PTHxx010	3.3 V/5 V 12 V	15 A 12 A	•	•	•	•	•	•	•	
PTHxx020	3.3 V/5 V 12 V	22 A 18 A	•	•	•	•	•	•	•	•
PTHxx030	3.3 V/5 V 12 V	30 A 26 A	•	•	•	•	•	•	•	•

Table 1 - Operating Features by Series and Input Bus Voltage

RoHS Compliance Ordering Information

PTH03020WAST



To order Pb-free (RoHS compatible) surface-mount parts replace the mounting option 'S' with 'Z', e.g. PTH03020WAZT. To order Pb-free (RoHS compatible) through-hole parts replace the mounting option 'H' with 'D', e.g. PTH03020WADT.



^{*}Auto-track™ is a trade mark of Texas Instruments

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2. System Interface Information

2.1 Input Capacitor

The recommended input capacitor(s) is determined by the 1,000 $\mu F^{(1)}$ minimum capacitance and 700 mA rms minimum ripple current rating. Ripple current and <100 m Ω equivalent series resistance (ESR) values are the major considerations, along with temperature, when designing with different types of capacitors. Unlike polymer tantalum, conventional tantalum capacitors have a recommended minimum voltage rating of 2 x (maximum dc voltage + ac ripple). This is standard practice to insure reliability. For improved ripple reduction on the input bus, ceramic capacitors may be substituted for electrolytic types using the minimum required capacitance.

2.2 Output Capacitance (Optional)

For applications with load transients (sudden changes in load current), regulator response will benefit from an external output capacitance. The recommended output capacitance of 330 μF will allow the module to meet its transient response specification (see product datasheet). For most applications, a high quality computergrade aluminum electrolytic capacitor is most suitable. These capacitors provide adequate decoupling over the frequency range, 2 kHz to 150 kHz, and are suitable when ambient temperatures are above 0 °C. For operation below 0 °C, tantalum, ceramic or Os-Con type capacitors are recommended. When using one or more nonceramic capacitors, the calculated equivalent ESR should be no lower than 4 m Ω (7 m Ω using the manufacturer's maximum ESR for a single capacitor). A list of preferred low-ESR type capacitors are identified in Table 2.

2.2.1 Tantalum Capacitors

Tantalum type capacitors can be used at both the input and output, and are recommended for applications where the ambient operating temperature can be less than 0 °C. The AVX TPS, Sprague 593D/594/595 and Kemet T495/T510 capacitor series are suggested over many other tantalum types due to their higher rated surge, power dissipation, and ripple current capability. As a caution many general purpose tantalum capacitors have considerably higher ESR, reduced power dissipation and lower ripple current capability. These capacitors are also less reliable when determining their power dissipation and surge current capability. Tantalum capacitors that do not have a stated ESR or surge current rating are not recommended for power applications.

When specifying Os-Con and polymer tantalum capacitors for the output, the minimum ESR limit will be encountered well before the maximum capacitance value is reached.

2.2.2 Ceramic Capacitors

Above 150 kHz the performance of aluminum electrolytic capacitors becomes less effective. To further improve the reflected input ripple current or the output transient response, multilayer ceramic capacitors can also be added. Ceramic capacitors have very low ESR and their resonant frequency is higher than the bandwidth of the regulator. When used on the output their combined ESR is not critical as long as the total value of ceramic capacitance does not exceed 300 μF . Also, to prevent the formation of local resonances, do not place more than five identical ceramic capacitors in parallel with values of 10 μF or greater.

2.2.3 Capacitor Table

Table 2 identifies the characteristics of capacitors from a number of vendors with acceptable ESR and ripple current (rms) ratings. The recommended number of capacitors required at both the input and output buses is identified for each capacitor type.

This is not an extensive capacitor list. Capacitors from other vendors are available with comparable specifications. Those listed are for guidance. The RMS ripple current rating and ESR (at 100 kHz) are critical parameters necessary to insure both optimum regulator performance and long capacitor life.

2.2.4 Designing for Very Fast Load Transients

The transient response of the dc-dc converter has been characterized using a load transient with a di/dt of 1 A/ μ s. The typical voltage deviation for this load transient is given in the datasheet specification table using the optional value of output capacitance. As the di/dt of a transient is increased, the response of a converter's regulation circuit ultimately depends on its output capacitor decoupling network. This is an inherent limitation with any dc-dc converter once the speed of the transient exceeds its bandwidth capability. If the target application specifies a higher di/dt or lower voltage deviation, the requirement can only be met with additional output capacitor decoupling. In these cases special attention must be paid to the type, value and ESR of the capacitors selected.

If the transient performance requirements exceed that specified in the datasheet, or the total amount of load capacitance is above 3,000 μF , the selection of output capacitors becomes more important.



VENDOR/ SERIES VOLTAGE VALUE MAX. ESR CURRENT AT SIZE (MM) EUROPE PART VOLTAGE VIDOR PART VOLTAGE VIDOR PART VOLTAGE VIDOR VOLTAGE VIDOR	CAPACITOR	CAPACITOR CHARACTERISTICS						ANTITY		
Aluminum FC (Radial) $10 \ V$ 560 $0.090 \ \Omega$ $0.090 \ \Omega$ $0.090 \ \Omega$ $1000 \ 0.068 \ \Omega$ $1000 \ 0.068 \ \Omega$ $1000 \ 0.060 \ \Omega$ $1000 \ 0.073 \ \Omega$ $1000 \ 0.075 \ \Omega$ $10000 \ 0.075 \ \Omega$ $1000000000000000000000000000000000000$	VENDOR/				CURRENT AT	SIZE (MM)		OUTPUT	PART	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	1									
FK (SMD)		10 V	560	0.090 Ω	755 mA	10.0 x 12.5	2	1	EEUFC1A561	
10 V 1000 0.080 Ω 850 mA 10.0 x 12.2 1 1 EEVFK1A102P						10.0 x 16.0	1	1		
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	FK (SMD)	l I								
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		10 V	1000	0.080 Ω	850 mA	10.0 x 12.2	1	1	EEVFK1A102P	
FX Os-con (Radial)	United Chemi-Con									
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	PXA (SMD)	6.3 V	470	$0.020~\Omega$	4130 mA	10.0 x 7.7	2 ⁽¹⁾	≤3	PXA6.3VC471MJ80TP	
10 V 1000 0.068 Ω 1050 mA 10.0 x 16.0 1 1 LXZ10VB102M10X16LL	FX Os-con (Radial)	6.3 V	1000	$0.013~\Omega$	4935 mA	10.0 x 10.5	1	≤2	6FX1000M	
Nichicon HD (Radial) 6.3 V 1000 0.053 Ω 1030 mA 10.0 x 12.5 1 1 UHD0J102MPR UPM1A102MPH6 Panasonic, Poly-Aluminum WA (SMD) 10 V 470 0.015 Ω 4500 mA 10.0 x 10.2 2(1) ≤3 EEFWA1A471P EEFSEUJ181R SANYO OS-Con SP (Radial) 10 V 470 0.015 Ω 24500 mA 10.0 x 10.5 2(1) ≤3 10SP470M SVP (SMD) 10 V 560 0.013 Ω 25200 mA 10.0 x 10.5 2(1) ≤3 10SP470M 10SVP560M 10 V 470 0.045 Ω 1723 mA 7.3 x 5.7 2(1) ≤5 TPSE477M010R0045 TPS (SMD) 10 V 470 0.060 Ω 1826 mA 7.3 x 5.7 2(1) ≤5 TPSV477M010R0060 TS20 10 V 330 0.040 Ω 1826 mA 7.3 x 4.3 3 ≤5 TS20X337M010AS T530 10 V 330 0.015 Ω 24200 mA 7.3 x 4.3 3 ≤5 T520X337M010AS T530 10 V 330 0.015 Ω 24200 mA 7.3 x 4.3 3 ≤5 T530X337M010AS T530 10 V 330 0.015 Ω 24200 mA 7.3 x 4.3 3 ≤5 T530X337M010AS T530 10 V 330 0.015 Ω 24200 mA 7.3 x 4.3 2(1) ≤2 T530X477M006AS T530X477M006A	LXZ (Radial)	10 V	680		760 mA	10.0 x 12.5	2			
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$		10 V	1000	$0.068~\Omega$	1050 mA	10.0 x 16.0	1	1	LXZ10VB102M10X16LL	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	Nichicon									
Panasonic, Poly-Aluminum WA (SMD) 10 V 470 0.017 Ω 4500 mA 10.0 x 10.2 $2^{(1)}$ ≤3 EEFWA1A471P EEFSE0J181R SANYO Os-Con SP (Radial) 10 V 470 0.015 Ω >4500 mA 10.0 x 10.5 $2^{(1)}$ ≤3 10SP470M SVP (SMD) 10 V 470 0.015 Ω >4500 mA 10.0 x 10.5 $2^{(1)}$ ≤3 10SP470M SVP (SMD) 10 V 560 0.013 Ω >5200 mA 10.0 x 12.7 2 ≤2 10SVP560M AVX Tantalum 10 V 470 0.045 Ω 1723 mA 7.3 x 5.7 $2^{(1)}$ ≤5 TPSE477M010R0045 TFS (SMD) 10 V 330 0.040 Ω 1826 mA 7.3 x 4.3 3 ≤5 TPSE477M010R0060 Kemet (SMD) 10 V 330 0.040 Ω 1800 mA 7.3 x 4.3 3 ≤5 T520X337M010AS T520 10 V 330 0.015 Ω 3800 mA 7.3 x 4.3 3 ≤5 T530X37M010AS T590 10 V 470	HD (Radial)	6.3 V	1000	$0.053~\Omega$	1030 mA	10.0 x 12.5	1	1	UHD0J102MPR	
Poly-Aluminum WA (SMD)	PM (Radial)	10 V	1000	$0.065~\Omega$	1060 mA	16.0 x 15.0	1	1	UPM1A102MPH6	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$,									
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$,	10 V	470	0.017.0	4500 mA	10 0 x 10 2	2(1)	<3	FFFWA1A471P	
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$	· ,	· ·	-							
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$										
$\begin{array}{c ccccccccccccccccccccccccccccccccccc$		10.1/	470	0.015.0	>4500 m∆	100 × 105	2(1)	<3	10SD470M	
AVX Tantalum	· '	· ·								
TPS (SMD) 10 V 470 0.060Ω 1826 mA 7.3×5.7 $2^{(1)}$ ≤ 5 TPSV477M010R0060 Kemet (SMD) 10 V 330 0.040Ω 1800 mA 7.3×4.3 3 ≤ 5 T520X337M010AS T530 10 V 330 0.015Ω >3800 mA 7.3×4.3 3 ≤ 3 T530X337M010AS T530 10 V 470 0.012Ω 4200 mA 7.3×4.3 3 ≤ 3 T530X337M010AS Vishay-Sprague 595D (SMD) 10 V 470 0.100Ω 1440 mA 7.2×6.0 $2^{(1)}$ ≤ 5 595D477X0010R2T 94SA (Radial) 16 V 1000 0.015Ω 9740 mA 16.0×25.0 1 ≤ 5 595D477X0010R2T 94SA (Radial) 16 V 10 0.002Ω 1210 case 1 ≤ 5 C1210C106M4PAC X5R (SMD) 6.3 V 47 0.002Ω 1210 case 1 ≤ 5 GRM32ER60J107M X5R (SMD) 6.3 V 47	` ′									
Kemet (SMD) T520 10 V 330 0.040 Ω 1800 mA 7.3 x 4.3 3 ≤5 T520X337M010AS T530 10 V 330 0.015 Ω >3800 mA 7.3 x 4.3 3 ≤3 T530X337M010AS T530 6.3 V 470 0.012 Ω 4200 mA 7.3 x 4.3 2(1) ≤2 T530X477M006AS Vishay-Sprague 595D (SMD) 10 V 470 0.100 Ω 1440 mA 7.2 x 6.0 2(1) ≤5 595D477X0010R2T 94SA (Radial) 16 V 1000 0.015 Ω 9740 mA 16.0 x 25.0 1 ≤3 94SA108X0016HBP Kemet, Ceramic, X5R (SMD) 16 V 10 0.002 Ω 1210 case 1 ≤5 C1210C106M4PAC X5R (SMD) 6.3 V 47 0.002 Ω 1210 case 1 ≤5 GRM32ER60J107M X5R (SMD) 6.3 V 47 10 0.002 Ω 1210 case 1 ≤5 GRM32ER60J107MT X5R (SMD) 6.3 V 100 0.002 Ω 1210		· ·				1	_		l I	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	TPS (SMD)	10 V	470	0.060 Ω	1826 mA	7.3 x 5.7	2(1)	≤5	TPSV477M010R0060	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Kemet (SMD)									
Vishay-Sprague 470 0.012 Ω 4200 mA 7.3 x 4.3 $2^{(1)}$ ≤2 T530X477M006AS Vishay-Sprague 595D (SMD) 10 V 470 0.100 Ω 1440 mA 7.2 x 6.0 $2^{(1)}$ ≤5 595D477X0010R2T 94SA (Radial) 16 V 1000 0.015 Ω 9740 mA 16.0 x 25.0 1 ≤3 94SA108X0016HBP Kemet, Ceramic, X5R (SMD) 16 V 10 0.002 Ω 1210 case 1 ≤5 C1210C106M4PAC X5R (SMD) 6.3 V 47 0.002 Ω 1210 case 1 ≤5 GRM32ER60J107M X5R (SMD) 6.3 V 47 3225 mm 1 ≤5 GRM32ER60J476M TDK, Ceramic X5R (SMD) 6.3 V 100 0.002 Ω 1210 case 1 ≤3 C3225X5R0J107MT X5R (SMD) 6.3 V 47 100 0.002 Ω 1210 case 1 ≤3 C3225X5R0J476MT		· ·								
Vishay-Sprague 10 V 470 0.100 Ω 1440 mA 7.2 x 6.0 $2^{(1)}$ ≤5 595D477X0010R2T 94SA (Radial) 16 V 1000 0.015 Ω 9740 mA 16.0 x 25.0 1 ≤3 94SA108X0016HBP Kemet, Ceramic, X5R (SMD) 16 V 10 0.002 Ω 1210 case 1 ≤5 C1210C106M4PAC X5R (SMD) 6.3 V 47 0.002 Ω 1210 case 1 ≤5 C1210C476K9PAC Murata, Ceramic X5R (SMD) 6.3 V 47 47 3225 mm 1 ≤5 GRM32ER60J107M X5R (SMD) 16 V 22 1 ≤5 GRM32ER60J476M TDK, Ceramic X5R (SMD) 6.3 V 100 0.002 Ω 1210 case 1 ≤3 C3225X5R0J107MT X5R (SMD) 6.3 V 47 47 1210 case 1 ≤3 C3225X5R0J476MT	T530									
$\begin{array}{cccccccccccccccccccccccccccccccccccc$		6.3 V	470	0.012 Ω	4200 mA	7.3 x 4.3	2(1)	≤2	T530X477M006AS	
94SA (Radial) 16 V 1000 0.015 Ω 9740 mA 16.0 x 25.0 1 ≤3 94SA108X0016HBP Kemet, Ceramic, X5R (SMD) 16 V 10 0.002 Ω 1210 case 3225 mm 1 ≤5 C1210C106M4PAC C1210C476K9PAC Murata, Ceramic X5R (SMD) 6.3 V 100 0.002 Ω 1210 case 3225 mm 1 ≤3 GRM32ER60J107M GRM32ER60J476M GRM32ER60J476M GRM32ER60J476M GRM32ER60J476M GRM32ER60J476M GRM32ER61C226K GRM32ER61C226K GRM32DR61C106K TDK, Ceramic X5R (SMD) 6.3 V 100 0.002 Ω 1210 case 3225 mm 1 ≤3 C3225X5R0J107MT GRMT GRMT GRMT GRMT GRMT GRMT GRMT GR	Vishay-Sprague									
Kemet, Ceramic, X5R (SMD) 16 V $\\ 6.3 \text{ V}$ 10 $\\ 47$ 0.002 Ω $\\ 0.002 \Omega$ 1210 case $\\ 3225 \text{ mm}$ 1 $\\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\ \\$		10 V	470	$0.100~\Omega$	1440 mA	7.2 x 6.0	2(1)		595D477X0010R2T	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	94SA (Radial)	16 V	1000	$0.015~\Omega$	9740 mA	16.0 x 25.0	1	≤3	94SA108X0016HBP	
$ \begin{array}{c ccccccccccccccccccccccccccccccccccc$	Kemet, Ceramic.	16 V	10	0.002 Ω		1210 case	1	<5	C1210C106M4PAC	
X5R (SMD)			-							
X5R (SMD)	Murata Caramio	631/	100	0.002.0		1210 0200	1	<3	GRM32FR60 I107M	
		' '		0.002 32						
16 V 10 ≤5 GRM32DR61C106K TDK, Ceramic X5R (SMD) 6.3 V 100 0.002 Ω 1210 case 1 3225 mm 1 ≤5 3 C3225X5R0J107MT 3225 mm 1 ≤5	7.511 (51415)					0220 111111				
TDK, Ceramic 6.3 V 100 0.002 Ω 1210 case 1 ≤3 C3225X5R0J107MT X5R (SMD) 6.3 V 47 3225 mm 1 ≤5 C3225X5R0J476MT		l I					, ,			
X5R (SMD) 6.3 V 47 3225 mm 1 ≤5 C3225X5R0J476MT	TDK Coronia			0.000.0		1010	4			
	1			0.002 \(\Omega\)						
	YOU (OINID)	l I				ا ااااا	-			
16 V 10 ≤5 C3225X5R1C106MT							'			

⁽¹⁾ Total capacitance of 940 μF is acceptable based on the combined ripple current rating.

Table 2 - Recommended Input/Output Capacitors



3. Mechanical Information

3.1 Mechanical Outline Drawings

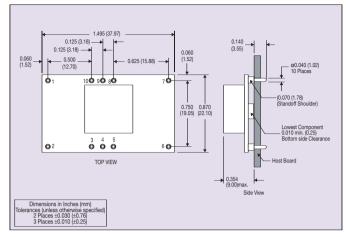


Figure 1 - Plated Through-Hole Mechanical Drawing

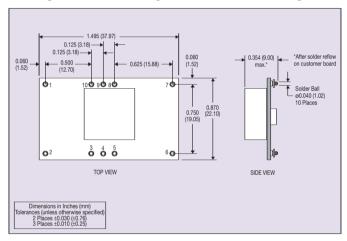


Figure 2 - Surface Mount Mechanical Drawing

3.2 Pin-out Table

PIN CONNECTIONS					
PIN NUMBER	FUNCTION				
1	Ground				
2	V _{in}				
3	Inhibit				
4	V _{o adjust}				
5	V _{o sense}				
6	V _{out}				
7	Ground				
8	Track				
9	Margin down				
10	Margin up				

Table 3 - Pin Connections

3.3 Pin Description

3.3.1 Ground

This is the common ground connection for the V_{in} and V_{out} power connections. It is also the 0 Vdc reference for the control inputs.

3.3.2 V_i

The positive input voltage power node to the module, which is referenced to common GND.

3.3.3 Inhibit

The Inhibit pin is an open-collector/drain negative logic input that is referenced to GND. Applying a low level ground signal to this input disables the module's output and turns off the output voltage. When the Inhibit control is active, the input current drawn by the regulator is significantly reduced. If the Inhibit pin is left open-circuit, the module will produce an output whenever a valid input source is applied.

3.3.4 V_o Adjust

A 0.1 W, 1% tolerance (or better) resistor must be connected between this pin and the GND pin to set the output voltage to the desired value. The set point range for the output voltage is from 0.8 V to 2.5 V. The resistor required for a given output voltage may be calculated from the following formula. If left open circuit, the module output will default to its lowest output voltage value.

$$R_{set} = 10 \text{K x} \frac{0.8 \text{V}}{\text{V}_{out} - 0.8 \text{V}} - 2.49 \text{ k}\Omega$$

The specification table gives the preferred resistor values for a number of standard output voltages.

3.3.5 V_o Sense

The sense input allows the regulation circuit to compensate for voltage drop between the module and the load. For optimal voltage accuracy $\rm V_o$ Sense should be connected to $\rm V_{out}$. It can also be left disconnected.

3.3.6 V_{out}

The regulated positive power output with respect to the GND node.

3.3.7 Track

This is an analog control input that enables the output voltage to follow an external voltage. This pin becomes active typically 20 ms after the input voltage has been applied, and allows direct control of the output voltage from 0 V up to the nominal set-point voltage. Within this range the output will follow the voltage at the Track pin on a volt-for-volt basis. When the control voltage is raised above this range, the module regulates at its set-point voltage. The feature allows the output voltage to rise simultaneously with other modules powered from the same input bus. If unused, the input should be connected to Vin. **Note:** Due to the under-voltage lockout feature, the output of the module cannot follow its own input voltage during power up. For more information, consult the related application note.

3.3.8 Margin Down

When this input is asserted to GND, the output voltage is decreased by 5% from the nominal. The input requires an open-collector (open-drain) interface. It is not TTL compatible. A lower percent change can be accommodated with a series resistor.

3.3.9 Margin Up

When this input is asserted to GND, the output voltage is increased by 5%. The input requires an open-collector (open-drain) interface. It is not TTL compatible. The percent change can be reduced with a series resistor.



4. Packaging Information

4.1 Packaging

The PTH03020 are available in trays of 15 units and tape and reel format in quantities of 150 units per reel. Tray dimensions including pick point are shown in Figure 4.

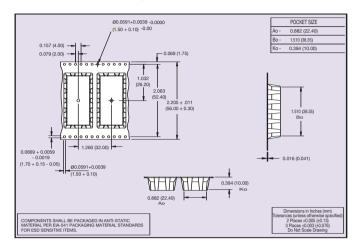


Figure 3 - Tape Dimensions

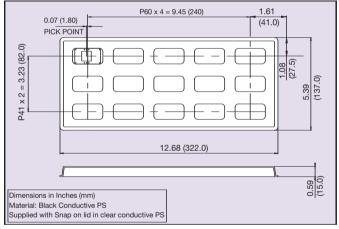


Figure 4 - Tray

4.2 Labeling and Part Numbering Sequence

All units in the series will be clearly marked to allow ease of identification for the end user. Figure 5 gives details of all the models.

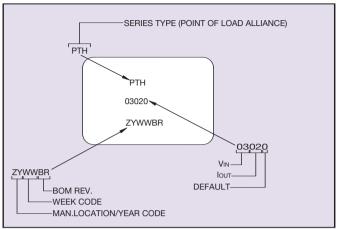


Figure 5 - PTH03020 Part Numbering

5. Safety Information

5.1 Safety Standards and Approvals

All models will have full international safety approval including EN60950 and UL/cUL1950. Models have been submitted to independent safety agencies for approval.

5.2 Fuse Information

Any suitable value fuse (based on the input ratings) maybe used in the unearthed input line. However this is not required for compliance with safety.

5.3 Safety Considerations

The converter must be installed as per guidelines outlined by the various safety agency approvals, if safety agency approval is required for the overall system.



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6. Operating Information

6.1 Overtemperature Protection (OTP)

Only the PTHxx020 and PTHxx030 series of products have overtemperature protection. These products have an on-board temperature sensor that protects the module's internal circuitry against excessively high temperatures. A rise in the internal temperature may be the result of a drop in airflow, or a high ambient temperature. If the internal temperature exceeds the OTP threshold (see datasheet specifications), the module's Inhibit control is automatically pulled low. This disables the regulator allowing the output voltage to drop to zero. (The external output capacitors will be discharged by the load circuit). The recovery is automatic, and begins with a soft-start power up. It occurs when the the sensed temperature decreases by about 10 °C below the trip point.

Note

The overtemperature protection is a last resort mechanism to prevent thermal stress to the regulator. Operation at or close to the thermal shutdown temperature is not recommended and will reduce the long-term reliability of the module. Always operate the regulator within the specified Safe Operating Area (SOA) limits for the worst-case conditions of ambient temperature and airflow.

6.2 Overcurrent Protection

For protection against load faults, all modules incorporate output overcurrent protection. Applying a load that exceeds the regulator's overcurrent threshold will cause the regulated output to shut down. Following shutdown a module will periodically attempt to recover by initiating a soft-start power-up. This is described as a "hiccup" mode of operation, whereby the module continues in the cycle of successive shutdown and power up until the load fault is removed. During this period, the average current flowing into the fault is significantly reduced. Once the fault is removed, the module automatically recovers and returns to normal operation.

6.3 Soft-Start Power-Up

The Auto-Track feature allows the power-up of multiple PTH modules to be directly controlled from the Track pin. However in a stand-alone configuration, or when the Auto-Track feature is not being used, the Track pin should be directly connected to the input voltage, Vin (see Figure 6).

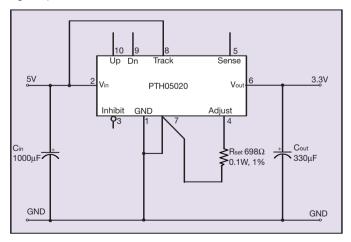
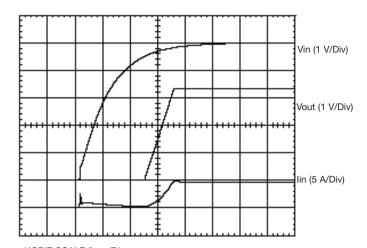


Figure 6 - Soft-Start Power-up

When the Track pin is connected to the input voltage the Auto-Track function is permanently disengaged. This allows the module to power up entirely under the control of its internal soft-start circuitry. When power up is under soft-start control, the output voltage rises to the set-point at a quicker and more linear rate.



HORIZ SCALE:5 ms/Div

Figure 7 - Power-up Characteristic

From the moment a valid input voltage is applied, the soft-start control introduces a short time delay (typically 5 ms to 10 ms) before allowing the output voltage to rise. The output then progressively rises to the module's setpoint voltage. Figure 6 shows the soft-start power-up characteristic of the 22 A output product (PTH05020W), operating from a 5 V input bus and configured for a 3.3 V output. The waveforms were measured with a 5 A resistive load, with Auto-Track disabled. The initial rise in input current when the input voltage first starts to rise is the charge current drawn by the input capacitors. Power-up is complete within 15 ms.



7. Feature Set

7.1 Adjusting the Output Voltage

The $\rm V_{\rm o}$ adjust control (pin 4) sets the output voltage of the PTH03020 product. The adjustment range is from 0.8 Vdc to 2.5 Vdc. The adjustment method requires the addition of a single external resistor, $\rm R_{\rm set}$, that must be connected directly between the Vo Adjust and GND pins⁽¹⁾. Table 4 gives the preferred value for the external resistor for a number of standard voltages, along with the actual output voltage that this resistance value provides.

For other output voltages the value of the required resistor can either be calculated using the following formula, or simply selected from the range of values given in Table 5. Figure 8 shows the placement of the required resistor.

$$R_{set} = 10K \times \frac{0.8V}{V_{out} - 0.8V} - 2.49 \text{ k}\Omega$$

V _{out} Standard	R _{set} (Preferred Value)	V _{out} (Actual)
2.5 V	2.21 kΩ	2.502 V
2.0 V	4.12 kΩ	2.010 V
1.8 V	5.49 kΩ	1.803 V
1.5 V	8.87 kΩ	1.504 V
1.2 V	17.4 kΩ	1.202 V
1.0 V	36.5 kΩ	1.005 V
0.8 V	Open	0.8 V

Table 4 - Preferred Values of R_{set} for Standard Output Voltages

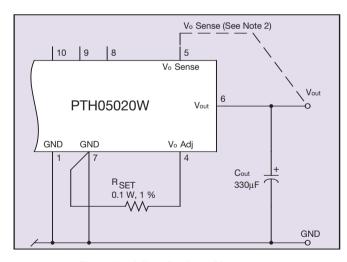


Figure 8 - Adjust Resistor Placement

OUTPUT VOLTAGE SET-POINT RESISTOR VALUES							
Va Req'd	Rset	Va Req'd	Rset	Va Req'd	Rset		
0.800	Open	1.225	16.3 kΩ	1.75	5.93 kΩ		
0.825	318 kΩ	1.250	15.3 kΩ	1.80	5.51 kΩ		
0.850	158 kΩ	1.275	14.4 kΩ	1.85	5.13 kΩ		
0.875	104 kΩ	1.300	13.5 kΩ	1.90	4.78 kΩ		
0.900	77.5 kΩ	1.325	12.7 kΩ	1.95	4.47 kΩ		
0.925	61.5 kΩ	1.350	12.1 kΩ	2.00	4.18 kΩ		
0.950	50.8 kΩ	1.375	11.4 kΩ	2.05	3.91 kΩ		
0.975	43.2 kΩ	1.400	10.8 kΩ	2.10	3.66 kΩ		
1.000	37.5 kΩ	1.425	10.3 kΩ	2.15	3.44 kΩ		
1.025	33.1 kΩ	1.450	9.82 kΩ	2.20	3.22 kΩ		
1.050	29.5 kΩ	1.475	9.36 kΩ	2.25	3.03 kΩ		
1.075	26.6 kΩ	1.50	8.94 kΩ	2.30	2.84 kΩ		
1.100	24.2 kΩ	1.55	8.18 kΩ	2.35	2.67 kΩ		
1.125	22.1 kΩ	1.60	7.51 kΩ	2.40	2.51 kΩ		
1.150	20.4 kΩ	1.65	6.92 kΩ	2.45	2.36 kΩ		
1.175	18.8 kΩ	1.70	6.4 kΩ	2.50	2.22 kΩ		
1.200	17.5 kΩ						

Notes:

- 1 Use a 0.1 W resistor, with a tolerance of 1% (or better). Place the resistor as close to the regulator as possible. Connect the resistor directly between pins 4 and 7 using dedicated PCB traces.
- $2\,$ Never connect capacitors from V $_{\rm o}$ Adjust to either GND or V $_{\rm out}.$ Any capacitance added to the V $_{\rm o}$ Adjust pin will affect the stability of the regulator.

Table 5 - Output Voltage Set-point Resistor Values

7.2 Output ON/OFF Inhibit

For applications requiring output voltage ON/OFF control,each series of the PTH family incorporates an output Inhibit control pin. The inhibit feature can be used wherever there is a requirement for the output voltage from the regulator to be turned OFF.

The power modules function normally when the Inhibit pin is left open-circuit, providing a regulated output whenever a valid source voltage is connected to V_{in} with respect to GND. Figure 9 shows the typical application of the inhibit function. Note the discrete transistor (Q1). The Inhibit control has its own internal pull-up to +Vin potential. An open-collector or open-drain device is recommended to control this input.

Turning Q1 on applies a low voltage to the Inhibit control pin and disables the output of the module. If Q1 is then turned off, the module will execute a soft-start power-up sequence. A regulated output voltage is produced within 20 ms. Figure 10 shows the typical rise in both the output voltage and input current, following the turnoff of Q1. The turn off of Q1 corresponds to the rise in the waveform, Q1 V_{DS}. The waveforms were measured with a 5 A load.



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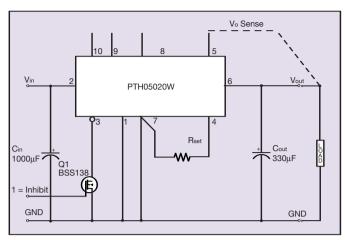


Figure 9 - Typical Application of the Inhibit Function

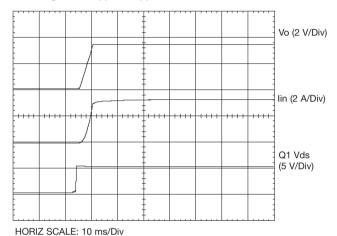


Figure 10 - Typical Rise in Output Voltage and Input Current

7.3 Pre-Bias Startup Capability

Only selected products in the PTH family incorporate this capability. Consult Table 1 to identify which product series are compliant.

In complex digital systems an external voltage can sometimes be present at the output of the module during power up. This voltage may be backfed through a dual supply logic component, such as an FPGA or ASIC. Another path might be via a clamp diode (to a lower supply voltage) as part of a power-up sequencing implementation.

Although the PTH family of modules can sink current under steadystate operating conditions, those that incorporate this capability will not do so during the soft-start cycle⁽¹⁾, or whenever the Inhibit pin is held low. However, to ensure the satisfactory operation of this feature certain conditions must be maintained during the application of input power⁽²⁾.

Note

The pre-bias start-up feature is not compatible with Auto-Track™. This is because when the module is under Auto-Track™ control, it is fully active and will sink current if the output voltage is below that of a back-feeding source. Therefore to ensure a pre-bias hold-off, one of the following two techniques must be followed when input power is first applied to the module. The Auto-Track™ function must either be disabled⁽³⁾, or the module's output held off using the Inhibit pin. The latter allows Auto-Track's internal RC charge ramp to rise above the setpoint voltage.

Notes:

- 1 The soft-start cycle is a relatively short period (up to 20 ms) that immediately follows either the application of a valid input source voltage, or the release of a ground signal at the Inhibit pin
- 2 To ensure that the regulator does not sink current when power is first applied (even with a ground signal applied to the Inhibit control pin), the input voltage <u>must</u> always be greater than the output voltage <u>through-out</u> the power-up and power-down sequence.
- 3 The Auto-Track™ function can be disabled at power up by immediately applying a voltage to the module's Track pin that is greater than its set-point voltage. This can be easily accomplished by pulling the Track pin up to V_{in} through a 1 kΩ resistor.

7.4 Margin Up/Down Controls

The PTHxx060W, PTHxx010W, PTHxx020W, and PTHxx030W module series incorporate Margin Up and Margin Down control inputs. These controls allow the output voltage set point to be momentarily adjusted¹, either up or down, by a nominal 5%. This provides a convenient method for dynamically testing the operation of the load circuit over its power supply margin or range. The $\pm 5\%$ change is applied to the adjusted output voltage as set by the external resistor, $R_{\mbox{set}}$ at the $V_{\mbox{O}}$ Adjust pin.

The 5% adjustment is made by driving the appropriate margin control input directly to the GND terminal⁽²⁾. A low-leakage opendrain device, such as a MOSFET or p-channel JFET is recommended for this purpose. Adjustments of less than 5% can also be accommodated by adding series resistors to the control inputs (See Figure 11). The value of the resistor can be selected from Table 6 or calculated using the following formula.

7.4.1 Up/Down Adjust Resistance Calculation

To reduce the margin adjustment to something less than 5%, series resistors are required (See R_{D} and R_{U} in Figure 11). For the same amount of adjustment, the resistor value calculated for R_{D} and R_{U} will be the same. The formulas is as follows:

$$R_u \text{ or } R_d = \frac{499}{\Lambda\%} - 99.8 \text{ k}\Omega$$

Where Δ % = The desired amount of margin adjust in percent.

Notes

- 1 The Margin Up and Margin Down controls were not intended to be activated simultaneously. If they are their affects on the output voltage may not completely cancel, resulting in the possibility of a slightly higher error in the output voltage set point.
- 2 The ground reference should be a direct connection to the module GND at pin 7 (pin 1 for the PTHxx050). This will produce a more accurate adjustment at the load circuit terminals. The transistors Q1 and Q2 should be located close to the regulator.
- 3 The Margin Up and Margin Dn control inputs are not compatible with devices that source voltage. This includes TTL logic. These are analog inputs and should only be controlled with a true opendrain device (preferably a discrete MOSFET transistor). The device selected should have low off-state leakage current. Each input sources 8 μA when grounded, and has an open-circuit voltage of 0.8 V.



% ADJUST	R_U/R_D
5	0.0 kΩ
4	24.9 kΩ
3	66.5 kΩ
2	150.0 kΩ
1	397.0 kΩ

Table 6 - Margin Up/Down Resistor Values

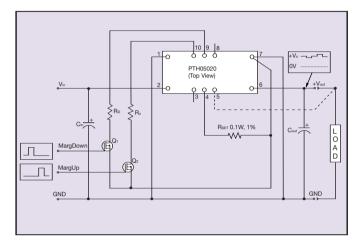


Figure 11 - Margin Up/Down Application Schematic

7.5 Remote Sense

The PTHxx010W, PTHxx020W, and PTHxx030W products incorporate an output voltage sense pin, $\rm V_o$ Sense. The $\rm V_o$ Sense pin should be connected to $\rm V_{out}$ at the load circuit (see datasheet standard application). A remote sense improves the load regulation performance of the module by allowing it to compensate for any 'IR' voltage drop between itself and the load. An IR drop is caused by the high output current flowing through the small amount of pin and trace resistance. Use of the remote sense is optional. If not used, the Vout Sense pin can be left opencircuit. An internal low-value resistor (15 Ω or less) is connected between the $\rm V_o$ Sense and $\rm V_{out}$, ensures that the output voltage remains in regulation.

With the sense pin connected, the difference between the voltage measured directly between the V_{out} and GND pins, and that measured from $V_{out\,sense}$ to GND, is the amount of IR drop being compensated by the regulator. This should be limited to a maximum of 0.3 V.

Note: The remote sense feature is not designed to compensate for the forward drop of non-linear or frequency dependent components that may be placed in series with the converter output. Examples include OR-ing diodes, filter inductors, ferrite beads, and fuses. When these components are enclosed by the remote sense connection they are effectively placed inside the regulation control loop, which can adversely affect the stability of the regulator.

8. Thermal Information

8.1 Thermal Reference Points

The electrical operating conditions namely:

- Input voltage, V_{in}
- Output voltage, V_o
- Output current, I_o

determine how much power is dissipated within the converter. The following parameters further influence the thermal stresses experienced by the converter:

- Ambient temperature
- · Air velocity
- · Thermal efficiency of the end system application
- · Parts mounted on system PCB that may block airflow
- · Real airflow characteristics at the converter location

8.2 Safe Operating Area Curve

Thermal characterisation data is presented in the datasheet in a safe operating area curve format which is repeated here in Figure 12. This SOA curve shows the load current versus the ambient air temperature and velocity.

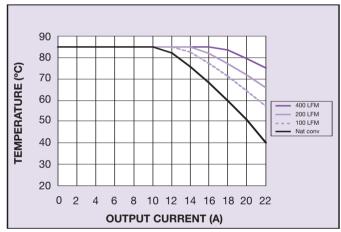


Figure 12 - Safe Operating Curve PTH03020W V_{out} = 2.5 V

8.3 Thermal Test Set-up

All of the data was taken with the converter soldered to a test board which closely represents a typical application. The test board is a 1.6 mm, eight layer FR4 PCB with the inner layers consisting of 2 oz power and ground planes. The top and bottom layers contain a minimal amount of metalisation. A board to board spacing of 1 inch was used. The data represented by the 0 m/s curve indicate a natural convection condition i.e. no forced air. However, since the thermal performance is heavily dependent upon the final system application, the user needs to ensure the thermal reference point temperatures are kept within the recommended temperature rating. It is recommended that the thermal reference point temperatures are measured using either AWG #36 or #40 gauge thermocouples or an IR camera. In order to comply with stringent Artesyn de-rating criteria, the ambient temperature should never exceed 85 °C. Please contact Artesyn Technologies for further support.



9. Use in a Manufacturing Environment

9.1 Recommended Land Pattern

It is recommended that the customer uses a solder mask defined land pattern similar to that shown in Figures 13 and 13.

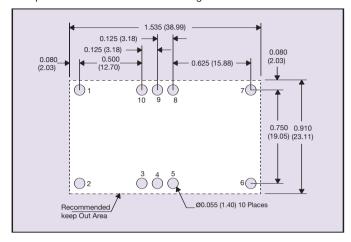


Figure 13 - Recommended Land Pattern (Through - Hole Model)

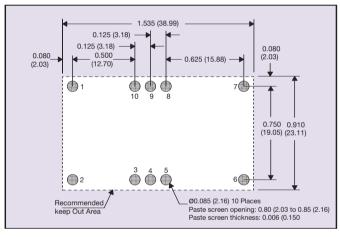


Figure 14 - Recommended Land Pattern (Surface-Mount Model)

Power pin connection should utilize four or more vias to the interior power plane of 0.025 (0.63) I.D. per input, ground and output pin (or the electrical equivalent).

As a surface-mount power component, interconnection to internal power planes will typically be required. This is accomplished by placing a number of vias between the SMT pad and the relevant plane. the number and exact location of these vias should be determined based on electrical resistivity, current flow and thermal requirements.

10. Auto-Track™

10.1 Auto-Track™ Function

The Auto-Track™ function is unique to the PTH family, and is available with the all "Point-of-Load Alliance" (POLA) products. Auto-Track was designed to simplify the amount of circuitry required to make the output voltage from each module power up and power down in sequence. The sequencing of two or more supply voltages during power up is a common requirement for complex mixed-signal applications, that use dual-voltage VLSI ICs such as DSPs, micro-processors, and ASICs.

10.2 How Auto-Track™ Works

Auto-Track™ works by forcing the module's output voltage to follow a voltage presented at the Track control pin. This control range is limited to between 0 V and the module's set-point voltage. Once the track-pin voltage is raised above the set-point voltage, the module's output remains at its set-point(¹). As an example, if the Track pin of a 2.5 V regulator is at 1 V, the regulated output will be 1 V. But if the voltage at the Track pin rises to 3 V, the regulated output will not go higher than 2.5 V.

As the regulated output from the module simply follows the voltage at the Track pin, it is able to 'track' virtually any voltage source during the power-up sequence⁽²⁾. This can be the rising voltage of an externally generated master ramp waveform, or the output voltage from another power supply circuit⁽³⁾. For convenience, each Track pin is also provided with an internal RC charge circuit that can produce a compatible voltage ramp from the input source voltage.

10.3 Typical Application

The simplest implementation of Auto-Track™ is to connect the Track control pins of two or more compliant PTH modules together. This forces the Track pins of the modules to follow the same collective internal RC ramp waveform, and also allows them to be controlled through a single transistor or switch.

To initiate a power-up sequence, it is recommended that the Track control be first pulled to ground potential. This should be done at or before input power is applied to the modules, and then held for at least 20 ms⁽⁴⁾ thereafter. This brief period gives the modules time to complete their internal soft-start initialization. Applying a logic level high signal to the circuit's ON/0FF Control turns Q1 on and applies a ground signal to the Track pins. After completing their internal soft-start intialization, the output of all modules will remain at zero volts while Q1 is on.

20 ms after a valid input voltage has been applied to the modules, Q1 may be turned off. This allows the track control voltage to automatically rise toward to the modules' input voltage. During this period the output voltage of each module will rise in unison with other modules, to its respective set-point voltage.

Figure 16 shows the output voltage waveforms from the circuit of Figure 15 after the ON/OFF Control is set from a high to a low-level voltage. The waveforms, V_01 and V_02 represent the output voltages from the two power modules, U1 (3.3 V) and U2 (2.0 V) respectively. V_01 and V_02 are shown rising together to produce the desired simultaneous power-up characteristic.



The same circuit also provides a power-down sequence. Power down is the reverse of power up, and is accomplished by lowering the track control voltage back to zero volts. The important constraint is that a valid input voltage must be maintained until the power down is complete. It also requires that Q1 be turned off relatively slowly. This is so that the Track control voltage does not fall faster than Auto-Track's slew rate capability, which is 5 V/ms. The components R1 and C1 in Figure 15 limit the rate at which Q1 can pull down the Track control voltage. The values of 100 $\mathrm{k}\Omega$ and 0.047 $\mathrm{\mu}\mathrm{F}$ correlate to a decay rate of about 0.6 V/ms.

The power-down sequence is initiated with a low-to-high transition at the On/Off Control input to the circuit. Figure 17 shows the power-down waveforms. As the Track control voltage falls below the nominal set-point voltage of each power module, then its output voltage decays with all the other modules under Auto-Track™ control.

Notes on the of Use Auto-Track™

- 1 The Track pin voltage must be allowed to rise above the module's set-point voltage before the module can regulate at its adjusted set-point voltage.
- 2 The Auto-Track™ function will track almost any voltage ramp during power up, and is compatible with ramp speeds of up to 1 V/ms.
- 3 The absolute maximum voltage that may be applied to the Track pin is $V_{\rm in}$.
- 4 The module output will not follow the voltage at the Track pin until the module has completed its soft-start cycle. The soft start-cycle takes up to about 20 ms to complete. During this time it is recommended that the Track pin be held at ground potential.
- 5 After the soft-start sequence is complete, the module is capable of both sinking and sourcing current when following the voltage at the Track pin.

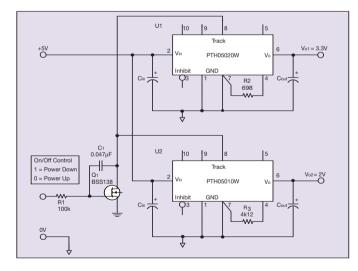
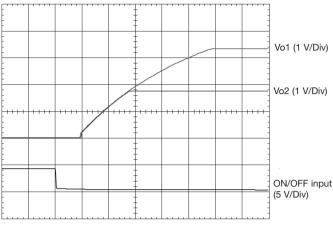


Figure 15 - Sequenced Power Up and Power Down Using Auto-Track™



HORIZ SCALE: 10 ms/Div

Figure 16 - Power Up with Auto-Track Control

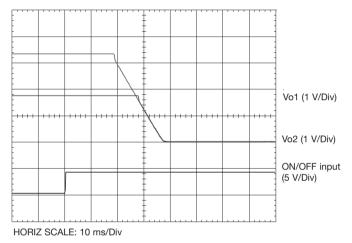


Figure 17 - Power Down with Auto-Track Control

The pre-bias start-up feature is not compatible with Auto-Track[™]. This is because when the module is under Auto-Track[™] control, it is fully active and will sink current if the output voltage is below that of a back-feeding source. Therefore to ensure a pre-bias hold-off, one of the following two techniques must be followed when input power is first applied to the module. The Auto-Track[™] function must either be disabled, or the module's output held off using the Inhibit pin.

The Auto-Track[™] function can be disabled at power up by immediately applying a voltage to the module's Track pin that is greater than its set-point voltage. This can be easily accomplished by pulling the Track pin up to Vin through a 1 k Ω resistor.

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